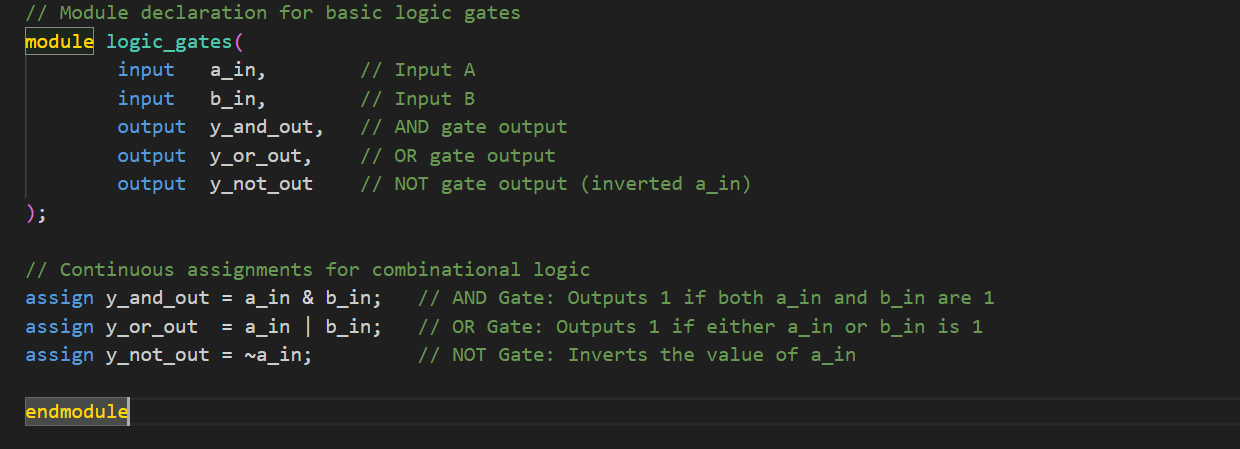
**Logic Gates Using Verilog HDL**

This Verilog code demonstrates the implementation of basic **logic gates**—AND, OR, and NOT. Logic gates are the fundamental building blocks of digital circuits, performing basic logical functions essential for digital computation.

**Module Description:**

The module is named logic\_gates and has:

* **Inputs:**
  + a\_in (Input A)
  + b\_in (Input B)
* **Outputs:**
  + y\_and\_out (Output of AND gate)
  + y\_or\_out (Output of OR gate)
  + y\_not\_out (Output of NOT gate applied to a\_in)
* **Code Explanation:**



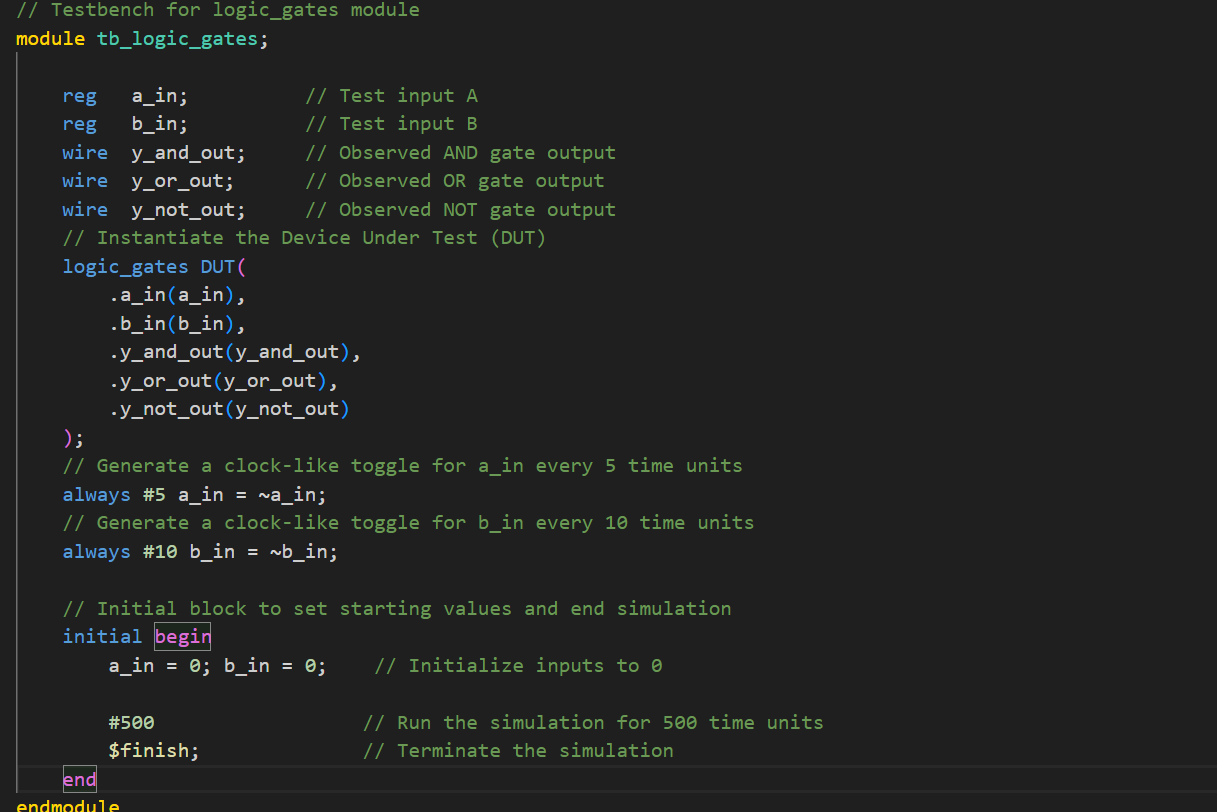
* **assign Statement:**  
  Used for continuous assignments in combinational logic.
* **Gate Operations:**
  + & → **AND Gate:** Outputs 1 only if both a\_in and b\_in are 1.
  + | → **OR Gate:** Outputs 1 if at least one input is 1.
  + ~ → **NOT Gate:** Inverts the value of a\_in.

**Truth Table:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **a\_in** | **b\_in** | **y\_and\_out (AND)** | **y\_or\_out (OR)** | **y\_not\_out (NOT a\_in)** |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 1 | 1 | 1 | 0 |

**Testbench for Logic Gates**

To verify the functionality of the logic\_gates module, we use a **testbench**. A testbench is a simulation environment used to apply test vectors to the design and observe the outputs.



* **Testbench Components:**
  + **Registers (reg):** Declared for a\_in and b\_in to apply test values.
  + **Wires (wire):** Connected to outputs to observe the results.
  + **Instantiation:** The logic\_gates module is instantiated as DUT (Device Under Test).
* **Stimulus Generation:**
  + **always Blocks:** Toggle a\_in every 5 time units and b\_in every 10 time units to generate test patterns.
  + **initial Block:** Sets initial conditions and ends the simulation after 500 time units.
* **Simulation Control:**
  + **$finish** is used to stop the simulation after the desired time.

**Applications:**

* **AND Gate:** Digital circuits for condition checking.
* **OR Gate:** Alarm systems, control circuits.
* **NOT Gate:** Inverters, signal conditioning.